Active Pixel X-ray Sensor Technology Development for SMART-X Focal Plane

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Abstract

We describe the need for and benefits of a targeted program to develop Active Pixel Sensor (APS) detector technology for the focal plane Active Pixel Sensor Imager (APSI) array and Critical Angle Transmission (CAT) Grating Spectrometer readout (CATGS) of the SMART-X mission. We review the current state of active pixel X-ray sensor technology. We show how a properly planned program will develop this technology for SMART-X. We estimate the cost and schedule of a program that develops the sensor technology to an appropriate technology readiness level (TRL-5/6) by 2019.

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1 SMART-X: Science Goals & Sensor Requirements

SMART-X will observe a variety of cosmic X-ray sources from black holes and galaxies at high redshift z>6 , to clusters of galaxies both locally and as distant as they can be found, to supernova remnants in the Milky Way and nearby local group galaxies, to stars and star forming regions within our galaxy. SMART-X will trace the evolution through cosmic time of galaxies and their elements using X-ray imaging and spectroscopy. Significant technology development will be needed in this decade to prepare for this exciting new mission. Here we focus on technology development to enable the Wide Field Imaging Spectrometer (APSI) and the CAT Grating Spectrometer readout (CATGS).

The APSI provides a large field of view with excellent spatial and temporal resolution and moderate spectral resolution. The heart of the APSI is a >16 megapixel focal plane comprised of an array of X-ray photon-counting active pixel sensors (APS). The CATGS provides the imaging spectrometer readout needed for the CAT gratings that captures the dispersed X-ray spectrum and separates overlapping orders. It too consists of arrays of active pixel sensors optimized for the grating. We discuss a carefully planned technology development sequence that will advance the core sensor technology required for the APSI to Technology Readiness Level (TRL) 5/6 by 2019.

Baseline APSI AND CATGS requirements are listed in Table 1.1. The APSI fully samples the 0.5 arc second SMART-X point-spread function (PSF). Its large field of view and its moderate spectral resolution complement the smaller-field and higher-spectral resolution of the SMART-X microcalorimeter. The APSI's high-speed readout provides the time resolution and count rate capability required to exploit SMART-X's large collecting area. The CATGRS provides very high spectral resolution at low energies (< 2.0 keV) to complement the high energy performance of the microcalorimeter; with a pixel size and speed well matched to the grating dispersion and expected counting rates.

Table 1: SMART-X APSI / CATGS Requirements

Parameter	APSI	CATGS
Pixel Size	< 16 μm	< 16 μm
Quantum Efficiency	> 90% 0.3-6.0 keV > 10% 0.2 – 9.0 keV	> 90% 0.1 – 2.0 keV
Read Noise	< 4 e RMS	< 4 e RMS
Field of View/Length	> 20 arc minutes (array)	> 20 cm (array)
Time Resolution	10 msec (full frame) 1 ms(window)	10 msec (full frame)
Count Rate	100 ct/PSF/s	30 ct/LSF/s
Radiation Tolerance	10 years at L2	10 years at L2

The APS technology development program we describe below will yield concrete benefits for high-energy astrophysics in the longer term as well providing a solid technical basis for future even more capable devices.

2 Current X-ray Imaging Technology

2.1 The need for new X-ray imaging technology

State-of-the-art astronomical X-ray imagers all include silicon charge-coupled device (CCD) detectors. CCDs have a number of limitations, which render them undesirable (perhaps even unsuitable) for use in SMART-X. Most significantly, it is simply not practical to sample a >16 megapixel CCD focal plane at the very high rates (~100 frames/s or more) required by SMART-X within the power and mass constraints of a space-flight instrument. Second, CCDs are notoriously sensitive to radiation encountered in the space environment. A L2 based mission would suffer unacceptable degradation in energy resolution without massive shielding.

These limitations can be overcome with an emerging generation of imaging detectors generically called Active Pixel Sensors (APS). Architecturally, the principal difference between the CCD and the APS is that the CCD is inherently a serial output device, with all pixels in the array being read in series by one (or at most a few parallel) on-chip amplifiers. In a CCD the very small charge packet (10^2 – 10^3 electrons) generated by an X-ray photon must be transferred internally over macroscopic distances (~cm). The APS, in contrast, can have random access capability, and features an output amplifier in each pixel. APS have much greater tolerance (x10^3) to radiation encountered on orbit because there is no need to transfer charge over macroscopic distances. Therefore much less mass is required for radiation shielding. Moreover, the on-chip circuitry in most APS devices exploits modern CMOS design and fabrication characteristics that allow operation with much less power than is required by CCDs.

The high-speed readouts of APS also provide significant performance benefits. These include i) less optical light contamination per frame time, which allows thinner optical blocking filters and therefore provides much better photon detection efficiency at energies below 0.5 keV; ii) less photon pileup and higher photon arrival time resolution, advantages which are especially important given the SMART-X combination of large collecting area and small point response function; and iii) less dark signal per readout, allowing higher operating temperature and, in principle, simpler, cheaper instrument design.

2.2 The need for targeted technology development for astronomy

Commercial forces are driving development in many aspects of APS technology. Pixel size and noise level, for example, are being reduced for such applications. While scientific sensor development will capitalize on these trends, we believe that some essential requirements for astronomical sensors (especially in the X-ray band) can only be met through, targeted, publicly-sponsored technology development. These include the requirements for deep depletion, low leakage current (dark noise) and good radiation tolerance. We discuss the importance of these features below.

2.3 Active pixel sensor architectures & current implementations

Active pixel sensors now under development for scientific applications use one of two architectures. A monolithic sensor is fabricated from a single wafer of semiconductor material that contains both the photosensitive volume and the readout circuitry of each pixel. A hybrid sensor is comprised of two (or more) wafers that are fabricated separately and then bonded together. One wafer of a hybrid contains the photosensitive volume (the detector layer or tier) and another wafer contains the readout circuitry. Within these broad architectural categories, different active pixel sensors may be distinguished by both the detector design and by in-pixel readout circuitry. In this section we describe some representative implementations of scientific APS now in development.

2.3.1 Monolithic Sensors

2.3.1.1 Description, strengths & weaknesses

Monolithic sensors incorporate both the detection and sensing functions on a single wafer. Initially most commercial monolithic sensors were front-illuminated, which means that the sensing circuitry obscures some of the photosensitive volume from incoming radiation. Recently the advantages of back-illuminated sensors have been recognized for low light level performance and these are becoming the industry standard for monolithic sensors. The devices already show remarkably low readout noise, primarily because very low-capacitance sense nodes produce a large responsivity (change in sense-node voltage for a given signal level). As a result, downstream noise sources contribute relatively less noise referred to input. The current limitations of monolithic sensors are different for different implementations. Some sensors (e.g., Sarnoff) have relatively small depletion depth (~10 μm). Others (e.g. MPI) have relatively large pixel sizes (~100 μm) compared with SMART-X requirements.

2.3.1.2 Current Implementations

MPI DEPFET: The Depleted Field Effect Transistor (DEPFET[**5**,**6**]) sensor is a unique, monolithic APS developed by the Max Planck Institute's Semiconductor Laboratory in Munich, Germany. In many respects it is the most advanced X-ray APS developed to date. Noise levels of 3.5 electrons, RMS, have been reported and array sizes up to 256x256 pixels have been fabricated. Depletion depths of 450 μm have been achieved. DEPFET sensors are the leading candidate for the European ATHENA Wide Field Imager. However, the typical pixel size for DEPFET devices (75-100 μm) is large.

SAO/Sarnoff Monolithic CMOS: The Smithsonian Astrophysical Observatory, in collaboration with Sarnoff Corporation, is developing monolithic CMOS based imagers for X-ray astronomy. Initial samples of 3-transistor (3T) devices with 8μm pixels have achieved "Fano-limited" performance (i.e., spectral resolution limited by the ionization statistics of silicon rather than by detector artifacts) and <2 e^- RMS noise. Figure 3.1 shows an X-ray spectrum obtained with such

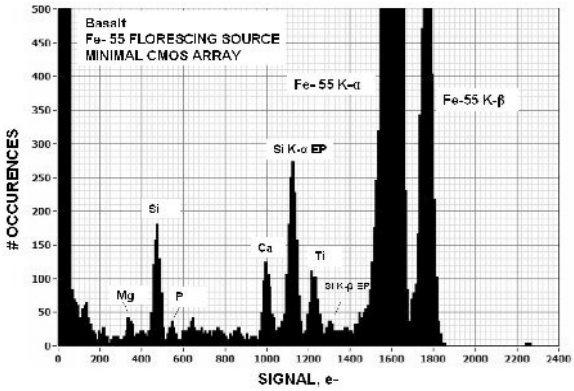

Figure 3.1: X-ray response of monolithic CMOS sensor from Sarnoff. Very low noise (<2 e^-, RMS) enables excellent resolution.

a device. Multiple sampling has reduced noise values to sub-electron values. A detailed description of these devices and the various pixel designs can be found in [**7**]. These preliminary devices have very high responsivity and are presently manufactured with low resistivity Si. The current material and CMOS fabrication process limit depletion depths to < 15 μm. Current 'test-bed' arrays have 512 x 512 pixels.

2.3.2 Hybrid Sensors

2.3.2.1 Description, strengths & weaknesses

Hybrid sensors locate the photo-absorption and charge sensing functions on separate wafers. One important advantage of the hybrid approach is the additional design freedom afforded for both detector and readout circuits. This allows the two parts of the sensor to be better optimized. A possible drawback of the hybrid approach is that the electrical interconnection between the two wafers can be relatively large, and may therefore increase the sense-node capacitance, reduce responsivity and increase read noise, but improved design of the interconnects can mitigate this effect while retaining the inherent advantages of the hybrid approach.

2.3.2.2 Current Implementations

Teledyne/PSU bump-bonded: Teledyne Imaging Sensors and Pennsylvania State University (PSU) have collaborated to develop bump-bonded, hybrid CMOS sensors for X-ray applications. These devices are derived from space-qualified IR detectors. They have been fabricated in 1024x1024 arrays with 18 μm pixel pitch, and similar detectors have been fabricated with pixel pitch of 10 μm. Versions of these detectors with 18 micron and 36 micron pitch have been tested with X-rays in the laboratory at PSU, and initial results, which show that they can be successfully used as sensitive X-ray detectors, can be found in [**8**]. Photodiode arrays have been made successfully with thicknesses of up to 200 μm.

These detectors can be read at speeds ranging from 100 kpix/s to 10 Mpix/s, for frame rates as high as 305 Hz using the 16 parallel outputs on the 1024x1024 test array. The same frame rate can be achieved for a new 4096x4096 array since it has more output lines. When operating at 100 kpix/s, read noise as low as 8 e- RMS for a single correlated double sample (CDS) frame and dark current of <0.01 e-/s/pixel (18 μm pixels) at 150 K has been achieved (Bongiorno, et al., Proc. SPIE, 7742,77420R, 2010). This noise can be lowered using non-destructive reads and/or by using an improved amplifier that is currently under development.

MIT Lincoln Laboratory three-dimensional circuit integration: MIT Lincoln Laboratory has developed fabrication technology that enables the dense vertical interconnection of multiple circuit layers[**9**]. For image sensor applications the first circuit layer or tier is a silicon or compound semiconductor device and the second and subsequent tiers contain silicon-on-insulator (SOI)-based electronics. Up to three interconnected tiers have been demonstrated to date. A cross-section of a three-dimensionally (3-D) integrated imager, obtained with a scanning electron microscope, is shown in Figure 3.2. The photodiode tier (Tier-1) consists of p+n diodes in high-resistivity (>3000 Ω-cm, n-type) float-zone silicon substrates. The readout tier (Tier-2) is fabricated using a fully depleted silicon-on-insulator (FDSOI) CMOS process. After the individual tiers have been fabricated, Tier-2 is mated to Tier-1 using a low-temperature oxide-oxide bonding process. A multistep dry-etch process forms 2-µm square 3-D-vias that serve as electrical interconnections between the tiers. At this point additional tiers could be bonded and interconnected. The detector tier is then thinned to approximately 50µm and the back-illuminated surface (the bottom surface in Figure 3.2) is passivated.

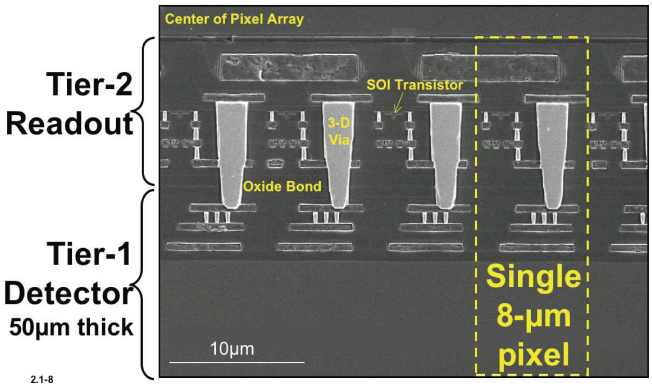

Figure 3.2: Cross-section of 3-D integrated hybrid CMOS sensor from MIT Lincoln Laboratory. Readout & detector arrays fabricated on separate tiers (wafers) are bonded and electrically connected using small (< 2 µm) 3-D vias. Vias & SOI readout transistors are indicated. Image from [**13**].

An X-ray sensitive three-dimensionally integrated APS fabricated with this process is discussed in [**10**]. Noise <13 e^- RMS, and spectral resolution of < 190 eV, FWHM at 5.9 keV have been achieved in a 50 µm thick, back-illuminated device. This technology provides a natural path to more highly integrated circuits, with analog-to-digital conversion and digital processing functions integrated with the detector package. Signal leads can be taken from the bottom of the sensor (i.e. from the side opposite that through which radiation enters) so that four-side-tileable detectors can be fabricated.

3 Technical challenges and approaches

Here we summarize areas in which future technical development is needed to meet SMART-X requirements. We have organized these development tasks into three categories that can be attacked in sequence. The first category includes pixel-level performance attributes, most of which pertain to the capability of a single pixel to detect a single X-ray photon and produce a measurable electrical signal containing sufficiently precise information about the photon energy, position, and time of arrival. Attributes in this category include pixel size; read noise; pixel rate; and detection and charge collection efficiency. The second category concerns development of the architecture and capabilities of a single focal plane chip or tile. Issues include chip-level power consumption, output architectures that enable adequate frame readout rate, and analog-to-digital conversion

capability in a device with format sufficiently large (at least 1 megapixel) to function as a single focal plane tile. In this category we also include flight qualification of a single tile to demonstrate tolerance for the vibration, thermal and radiation environments faced by a flight instrument. The final category includes attributes enabling production of the full-scale focal plane. Among these are mosaicing, advanced (in-focal-plane) digital processing to reduce and manage focal plane output data rate requirements, and flight qualification of a tiled focal plane.

3.1 Pixel-level development challenges

Read noise, responsivity and spectral resolution: Read noise is a critical determinant of X-ray spectral resolution. As discussed in Section 3 above, monolithic sensors have achieved noise levels commensurate with SMART-X requirements (2-4 e^- RMS), while the noise of hybrid sensors is currently a factor of 2-5 higher. The key to improved noise for hybrid sensors is to minimize sense-node capacitance within each pixel, thus increasing responsivity, and to optimize in-pixel amplifiers to reduce noise. This is a prime goal of current hybrid sensor development work.

High-energy quantum efficiency, Pixel size, and Aspect ratio: A depletion depth >145 μm in silicon is required to achieve SMART-X APSI requirements for high-energy (E > 5 keV) quantum efficiency. TIS hybrid X-ray sensors have demonstrated depletion depths of ~200 μm, already meeting the SMART-X needs. The LL hybrids have demonstrated ~50 μm depletion depth and extension to SMART-X requirements is probably straightforward. Among the monolithic sensors, MPE DEPFET devices have surpassed the SMART-X depletion depth requirement, but with large pixels. The Sarnoff monolithic sensors have depletion depths ~15 μm and current research aims to increase the depletion depth of these devices. The energy band requirement for the SMART-X grating spectrometer readout is less demanding than for the APSI and is likely to be within the reach of current technology monolithic CMOS.

Feature sizes in modern CMOS fabrication processes are quite small (< 0.35 μm), and in general fabrication of sufficiently small pixels (8 μm) is not a difficult challenge. A possible exception is the DEPFET technology, where a lower limit to the pixel size may currently lie at about 25 μm.

The SMART-X requirements for pixel size and depletion depth, taken together, pose another challenge to all sensor fabrication technologies. This aspect ratio (depth-to-width) is roughly a factor of 3 larger than has been achieved in current CCD detectors, and is likely to lead to greater charge diffusion between neighboring pixels. This problem can be solved by summing charge from neighboring pixels (as is routinely done with CCDs) but this process increases noise. Further development is required to understand and optimize the performance of pixels with such large aspect ratios.

Back-illumination and low-energy quantum efficiency: The back-illumination configuration, in which the photons enter the sensor from the side opposite the readout circuitry, is probably required to meet APSI quantum efficiency (QE) requirements, especially for soft X-rays (E < 1 keV). Good X-ray spectral resolution demands excellent charge-collection from the vicinity of the illuminated ('back') surface of the detector, since loss of even a few

percent of the photo-generated charge to surface recombination can degrade performance. Effective techniques for field control and passivation have recently been developed and applied to most types of APS with excellent demonstrated charge collection efficiency.

Readout rate, optical blocking, and low-energy quantum efficiency: The more rapid readout rates promised by APS architectures allow better photon arrival time resolution and lower probability of event pileup (two X-ray photons interacting within a single pixel within a single exposure). Equally importantly, faster readout allows better low-energy QE by reducing the probability that an out-of-band (UV or optical) photon will confuse the signal from an X-ray event. As a result, the optical depth of UV/optical blocking filters can be reduced, allowing better soft-X-ray QE. This effect can be quite significant: at 1 kHz frame rate, the reduction in blocking filter density compared to that required at CCD rates (~1Hz) would increase QE at 0.1 keV by almost an order of magnitude, particularly important for the CATGS.

In fact, the high frame rates envisioned for SMART-X require progress in all three development categories: at the pixel level, to ensure sufficiently low noise; at the tile level, to provide sufficient parallelism in the output circuitry; and at the focal plane level to deal with the large raw data rates produced by a >16 megapixel focal plane running at 100 frames/sec (>3.2 Gbytes/sec). Substantial progress has been achieved at the pixel level, but much work remains to be done at the tile- and focal-plane level to meet APSI or CATGS requirements. We discuss this further below.

3.2 Chip-level development challenges

Array size, frame-rate, output architecture and digitization: A key to achieving high frame rates with APS is proper design of chip- or tile-level output circuitry. Highly parallel architectures, with an output for each device column, are in principle possible. This circuitry may need to provide analog or digital signal processing to support noise-suppression techniques such as correlated double sampling. In practice the multiplexing of many channels to off-chip electronics may have to be done digitally, and would thus require near or on-chip digitization. Some of these capabilities are under development as separate, application-specific integrated circuits. A possible (but not necessarily required) step for SMART-X detector development will be to integrate these functions with the detector array. This will probably be done progressively, with array formats of increasing size.

3.3 Focal plane development challenges

Focal plane tiling: The SMART-X field of view requirement is sufficiently large that the focal plane must almost certainly be tiled with an array of devices. Moreover, the optimum focal surface of the Gen-X optic is not planar, so a mosaicked focal plane can provide better angular resolution for the observatory. Although the optimum size for each tile cannot yet be specified, it seems likely that individual devices comparable in size to current scientific CCDs (typically 25-50 mm square) may be used. It will be necessary to produce devices that can be tiled on at least 2 sides with minimal 'seam loss' (a 2 x 2 mosaic).

The technical challenge is to locate the necessary addressing, multiplexing, readout and processing circuitry and electrical connections, without wasting valuable field of view.

Hybrid sensors can solve this problem by placing the circuitry underneath the photosensitive layer. Packaging solutions for tile-able monolithic sensors beyond 2-sided mosaics have not yet been developed.

4 Technology Development Plan

4.1 Development strategy, technology gates and technical readiness

It is not clear at present which of the sensor architectures will best be able to meet SMART-X requirements, and we therefore believe that each type should be developed further in the near term, with the possibility that more than one will be needed.

We outline a program that addresses the three categories of APS technology development discussed in Section 3: pixel-level performance, chip-level performance and architecture, and focal plane-level development. A representative list of challenges in each category is presented in Table 4.1, along with our assessment of the current status. To make this assessment we compared the best results reported to date with nominal requirements for each parameter. We use a simple numerical rating scheme, assigning 0 if little or no work has yet been done to meet a requirement; 1 if some work has begun; 2 if we judge that a requirement may be met in a current development program; and 3 if a requirement has already been met. We intend these ratings to indicate the scope of development effort remaining to achieve corresponding performance targets.

The WFI technology development schedule is based on a series of technology gates, defined in Table 4.2, that are passed as related groups of performance targets are met. The gates also mark achievement of increasing technology readiness levels (TRL). Table 4.2 includes estimates of the number of sensor development cycles required to pass each gate, and an approximate date by which gates and the associated TRL may be achieved.

4.2 Assumptions, Schedule and Cost

We assume that single sensor development cycle (design, fabrication and test) requires three years. We assume three groups initially working in parallel, with one development cycle completed per architecture every 1.5-2 years and in some cases, we assume parallel cycles on given architecture.

Parameter	Development Target (Gen-X targets)	Sensor Family		
		JHU/Sarnoff	PSU/Teledyne	MIT/Lincoln
Pixel-level performance:				
Pixel Size	< 16 μm	3	3	3
Read Noise	< 4 e^- rms	3	2	2
Pixel Rate	1 Mpix/s	3	3	2
QE (@ 10 keV)	10% (>145 μm depletion)	1	3	2
QE (@ 0.1 keV)	10% (passivated surface)	1	3	2
Charge Collection	< 5% resolution loss	2	3	2
In-pixel CDS	subtract pixel baseline	3	1	3

Chip-level performance & architecture:				
Chip format	1-4 Megapixels	3	3	1
Pixel uniformity	<5% response variation	2	3	1
Power consumption	<50mW/cm^2	2	3	1
On-chip digitization	12 bits/pixel	1	0	1
Window rate	< 1 ms for 10x10 window	2	3	0
Flight qual.	Space qualification	0	1	0
Focal plane scaling & processing:				
Two-side tiling	< 300 μm seam loss	0	3	1
Processor integration	On-chip event identification	0	0	0
Focal plane qual.	Tolerate space environment	0	1	0
Code	0 = no progress to date	1=some work	2=may be met 1-2 years	3=already demonstrated

Note: a) See text for definition of numerical scale for development status.

Table 4.2: Gen-X WFI Technology Development Gates & Readiness Levels

Technology[a]		Requirements to be Met[b]	Development Cycles Needed/Date[c]		
Gate	TRL		Monolith (JHU)	3D Hybrid (MIT)	TIS Hybrid (PSU)
TG-1	3	Pixel size, noise & pixel rate	2/2015	2/2015	2/2015
		QE, charge collection, spectral resolution			
TG-2	4	Chip format & frame rate	2/2017	2/2017	2/2017
		On-chip digitization			
TG-3	5	Chip-level flight qualification	1/2019	1/2019	1/2019
TG-4	6	4-side tiling			
		Onboard processing/compression			
		Focal plane flight qualification	3/2021		

Notes: a) Upon completion;. b) See Table 4.1 for performance targets; c) FY achieved.

We assume that the targets within a given technology gate may be achieved in different sequences for different sensor architectures, and that selection of preferred architecture occurs by the time gate TG-3 is achieved.. After selection we assume parallel efforts that complete the remaining focal-plane-level development in three years.

TG-1 (TRL3) is achieved by the end of 2015. The first full-scale Smart-X tile is demonstrated in the laboratory by the end of 2017 (gate TG-2/TRL4). Flight qualification of a single tile sensor, as part of a sub-orbital payload or other mission, is expected by mid 2019 (TG-3/TRL 5). Focal plane-level development can begin in parallel with this in 2018. Qualification of a prototype focal plane should be feasible to reach TRL6 at TG-4 in 2021.

In total 18 development cycles are required, **at a total estimated cost of $27M** over 9 years. We derive the cost from our experience with currently funded APS development work at MIT, SAO and Penn State with FFRDC and commercial partners, that one development cycle costs roughly $1.5M (FY11). Costs by Fiscal year are shown in Table 4.3.

2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	**Total**
2.25	2.25	2.5	4.0	4	4.5	1.5	3.0	1.5	1.5	**27**

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